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10/079,988	02/20/2002	Ross V. La Fetra	100200334-1 6883		
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Intellectual Pro	perty Administration				
P.O. Box 272400			ART UNIT	PAPER NUMBER	
Fort Collins, CO 80527-2400			2133		

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Please find below and/or attached an Office communication concerning this application or proceeding.

14		Application	No.	Applicant(s)				
Office Action Summary		10/079,988		LA FETRA, ROSS V.				
		Examiner	niner Art Unit					
		Stephen M. E	Baker	2133				
Period fo	The MAILING DATE of this communication Reply	ion appears on the co	ver sheet with the c	orrespondence ad	idress			
THE - Exte after - If the - If NC - Failt Any	ORTENED STATUTORY PERIOD FOR MAILING DATE OF THIS COMMUNICA' nsions of time may be available under the provisions of 37 SIX (6) MONTHS from the mailing date of this communicate period for reply specified above is less than thirty (30) day of period for reply is specified above, the maximum statutor are to reply within the set or extended period for reply will, I reply received by the Office later than three months after the patent term adjustment. See 37 CFR 1.704(b).	TION. CFR 1.136(a). In no event, lation. ys, a reply within the statutory y period will apply and will expy statute, cause the application.	however, may a reply be tim y minimum of thirty (30) day: pire SIX (6) MONTHS from ion to become ABANDONEi	nely filed s will be considered timel the mailing date of this c D (35 U.S.C. § 133).				
Status								
1)⊠	Responsive to communication(s) filed or	n <u>05 <i>July</i> 2005</u> .						
2a)□	This action is FINAL . 2b)	☑ This action is non-	·final.					
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Disposit	ion of Claims							
5)□ 6)⊠ 7)□								
Applicat	ion Papers							
9)□	The specification is objected to by the Ex	caminer.						
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.								
	Applicant may not request that any objection							
11)	Replacement drawing sheet(s) including the The oath or declaration is objected to by				, ,			
Priority (under 35 U.S.C. § 119							
a)i	Acknowledgment is made of a claim for f All b) Some * c) None of: 1. Certified copies of the priority doc 2. Certified copies of the priority doc 3. Copies of the certified copies of the application from the International See the attached detailed Office action fo	uments have been rouments have been roughted been roughted by the priority documents Bureau (PCT Rule 1	eceived. eceived in Applications have been receive 7.2(a)).	on No ed in this National	Stage			
Attachmen	t(s)							
	e of References Cited (PTO-892)	4)	Interview Summary					
3) 🔲 Infori	e of Draftsperson's Patent Drawing Review (PTO-9 mation Disclosure Statement(s) (PTO-1449 or PTO r No(s)/Mail Date	/SB/08) 5)	Paper No(s)/Mail Da Notice of Informal P Other:		O-152)			

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Claim Rejections - 35 USC § 112

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

- 2. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 3. The specification as filed does not support the copying "without reading from and writing to an intermediate memory buffer" (sic - without writing to and reading from an intermediate memory) now recited by the independent claims. Page 9 is not specific regarding the path of copied data and, in conjunction with Fig. 3C, appears to imply that the copied data is read "by" the repeater and is thus presumably read into the repeater to enable the copying and then it is presumably written by (and from) the repeater into the spare. The copying operation is not described as involving materially different means than would be involved in any other combination of reading and writing operations. More specifically, the individual memory block read and write operations shown in FIGs. 3A, 3B, 3D, 3E and 3F all are understood to involve the generating (by the "repeater") of only a single address on a commonly-shared memory block address bus at any one time, in the standard manner, and so the same typical mode of access (one memory block address and one memory block enable at a time) presumably applies to all the memory block accesses shown in FIG. 3C. Moreover, the placement of the arrow (370) used to illustrate the "atomic read/write" operation in FIG. 3C

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evidently implies at least that the data to be copied to a memory bank is written "FROM REPEATER". If the repeater was not to be involved in the copying operation as observed herein by the examiner, it would presumably be necessary to provide a separate set of address lines and a separate set of read/write control lines to each memory block, which is apparently contradicted by the illustration of a simple common bus for all memory banks in FIGs. 3A-3F, not to mention being prominently absent from the written disclosure. Accordingly it should be evident that there is no support in the disclosure for the copying operation imagined by applicant's response to the rejection based on prior art and that the data repeater serves as an intermediate buffer for interblock copy operations.

Claim Rejections - 35 USC § 103

4. Claims 1-4 7-9, 12, 13 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,598,174 to Parks *et al* (hereafter Parks).

Parks discloses a storage device array "memory system" with arrangements for replacing a storage device that is about to fail with an unused spare storage device.

Data is striped across the storage devices in Parks' system, and so "a memory word is divided into said memory ...". Parks' system (Fig. 8) includes a hub "repeater". In a 'hot copy' process disclosed by Parks, client data accesses are not blocked while data is being copied from a "selected" failing (source) storage device into the spare (target) storage device (col. 4, line 8), and writes (Fig. 12) may be performed to both the failing device and the spare device (col. 4, lines 39-43) unless the affected location has not yet

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been copied (col. 19, lines 1-18). Parks thus discloses "configuring said memory system to perform write operations associated with said selected memory ... to both said selected memory ... and said spare memory ...". The 'hot copy' process involves "performing atomic read and write operations such that content of said selected memory ... is copied to said spare memory ...", with atomicity being provided by means of data lock algorithms (col. 19, lines 45-59). Read operations can be performed using the spare memory, if the data of the location to be read has already been copied to the spare memory (col. 19, lines 27-29). Such read operations, in addition to eventually removing the failing device in Parks' system, provide "configuring ... to redirect operations to be performed on said selected memory ... to said spare memory ...".

Although the storage devices can be semiconductor storage (col. 8, line 64), Parks does not describe such semiconductor storage devices as "memory banks".

Official Notice is taken that the usefulness of providing a semiconductor device unit in the form of a "bank", in a conventional manner, was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize Parks' semiconductor storage units as "banks". Such a realization would have been obvious because the usefulness of providing a semiconductor device unit in the form of a "bank", in a conventional manner, was already well known.

Although Parks states that the failing storage device can be removed while maintaining access to the non-failing devices (col. 3, lines 45-47), Parks does not specifically describe the replacing the failing storage device as "hot swapping". Official

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Notice is taken that the usefulness of replacing a failing storage unit by "hot swapping" (i.e. while the system is still running) was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement Parks' semiconductor storage units as "hot swappable" units. Such a realization would have been obvious because the usefulness of replacing a failing storage unit by "hot swapping" (i.e. while the system is still running) was already well known.

5. Claims 2, 10, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks as applied to claim 1 above, and further in view of U.S. Patent No. 5,357,509 to Ohizumi (hereafter Ohizumi.

Parks does not disclose copying the content of the spare storage device to the storage device that replaces the failing storage device after the failing device has been copied and replaced.

Ohizumi discloses copying the content of the spare storage device to the storage device that replaces the failing storage device after the failing device has been copied and replaced, providing the advantage that a spare device may then be re-used. It would have been obvious to a person having ordinary skill in the art to enhance Parks' storage system by providing for copying the content of the spare storage device to the storage device that replaces the failing storage device after the failing device has been copied and replaced. Such an enhancement would have been obvious because Ohizumi teaches that the advantage of a re-usable spare device is provided thereby.

Allowable Subject Matter

6. Claims 3-6, 11, 15 and 20 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed 05 July 2005 have been fully considered but they are not persuasive.

As noted above, support cannot be found for the invention as amended to define over the cited prior art.

Conclusion

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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